IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re application of:	§	Docket No.
	§	TSMC2003-0065/24061.508
Lin, et al.	§	
	§	Customer No. 42717
Serial No. 10/688,045	§	
	§	Group Art Unit: 1722
Filed: October 17, 2003	§	
	§	Examiner: Robert M. Kunemund
For: Fully Dry, Si Recess Free Process for Removing High K Dielectric Layer	§	
	§	
	§	

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Linda Ingram
Name

APPEAL BRIEF

In response to the Notice of Panel Decision from Pre-Appeal Brief Review dated September 15, 2006, Appellants submit this Appeal Brief in connection with an appeal from the final rejection of the Examiner, dated May 11, 2006, finally rejecting claims 1-40, all of the pending claims in this application.

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REAL PARTY IN INTEREST

The real party in interest is Taiwan Semiconductor Manufacturing Company, a Taiwanese company having a principal office and place of business at No. 8, Li-Hsin Rd. 6, Science-Based Industrial Park, Hsin-Chu, Taiwan 300-77, Taiwan R.O.C.

RELATED APPEALS AND INTERFERENCES

There are no related appeals and no related interferences regarding the above-identified patent application.

STATUS OF CLAIMS

Claims 1-40 are pending, stand finally rejected, and are on appeal here. Claims 1-40 are set forth in the Claims Appendix attached hereto.

STATUS OF AMENDMENTS AFTER FINAL REJECTION

No amendments have been made after the Final Office Action dated May 11, 2006.

SUMMARY OF THE CLAIM SUBJECT MATTER

The present invention, as set forth in independent claim 1, relates to a method of removing a high k dielectric layer from a substrate (paragraph 33, lines 1-3) comprising the steps of:

(a) providing a substrate with a high k dielectric layer formed thereon (paragraph 27, lines 1-3);

(b) depositing a gate layer and forming a gate electrode on said high k dielectric layer that exposes portions of said high k dielectric layer (paragraph 29, lines 1-4, Fig. 3); and

(c) etching through said exposed portions of said high k dielectric layer with a plasma etch comprised of

an inert gas,

BCl_3, and

one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4. (Fig. 3, paragraph 33, lines 1-19).

Another embodiment, as set forth in independent claim 20, relates to a method of forming a MOSFET (paragraph 26, lines 13-17), comprising:

(a) providing a substrate having shallow trench isolation features which separate active regions (paragraph 26, lines 5-9);

(b) forming a high k dielectric layer on said substrate (paragraph 27, lines 1-4);

(c) depositing a gate layer on said high k dielectric layer and etching through said gate layer to form a gate electrode and expose portions of said high k dielectric layer, said gate electrode is aligned over an active region (paragraph 29, lines 1-4, Fig. 3); and

(d) etching through exposed portions of said high k dielectric layer with a plasma etch comprised of

an inert gas,

BCl3, and

one or more fluorocarbon gases CXHYFZ,, wherein x and z are integers and y is an integer or is 0, or CH4. (Fig. 3, paragraph 33, lines 1-19, paragraph).

Another embodiment, as set forth in dependent claim 11, which further limits claim 1, requires that said plasma etch is performed with

BCl3,

an inert gas comprised of Ar, He, Ne, or Xe, and

one or more fluorocarbon gases including CF4, CHF3, CH2F2, CH3F, C2HF5, C2H2F4 and C2F6. (paragraph 33, lines 1-26).

Another embodiment, as set forth in dependent claim 29, which further limits independent claim 20, requires that said etching through exposed portions of said high k dielectric layer is performed with

BCl3,

an inert gas comprised of Ar, He, Ne, or Xe, and

one or more CXHYFZ gases including CF4, CHF3, CH2F2, CH3F, C2HF5, C2H2F4, and C2F6. (paragraph 33, lines 1-26).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1-40 stand rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 6,451,647 to Yang et al. ("Yang") in view of U.S. Patent No. 6,436,838 to Ying et al. ("Ying").

ARGUMENT

The issues for the Board's consideration are

I. Whether claims 1-40 are unpatentable under 35 U.S.C. §103(a) over Yang in view of Ying.

As detailed below, the Appellants believe that the Examiner has improperly applied the combination of references to the claims. More specifically, it is Appellants' belief that the Examiner cannot factually support a prima facie case of obviousness with respect to the rejected claims because the references, even when combined, fail to teach or suggest the claimed subject matter, and that the combination of references is improper.

Claims 1-40

Appellants traverse the rejection of these claims on the grounds that the references are defective in establishing a prima facie case of obviousness. It is well settled that, in order to reject a patent application for obviousness, the prior art reference must teach or suggest all of the claimed limitations. *In re Royka*, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). Moreover, all words in a claim must be considered in judging the patentability of that claim against the prior art. *In re Wilson*, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). Appellants respectfully submit that even if combined, Yang and Ying clearly do not teach or suggest the limitations of claim 1.

With respect to the improper application of Yang and Ying, the Appellants submit that neither Yang and Ying, separately or in combination, teach or suggest all of the elements of claim 1 as required by MPEP § 2143. Appellants traverse the rejection of this claim on the grounds that the references are defective in establishing a prima facie case of obviousness.

Claim 1 recites:

> A method of removing a high k dielectric layer from a substrate comprising the steps of:
>
> (a) providing a substrate with a high k dielectric layer formed thereon;
>
> (b) depositing a gate layer and forming a gate electrode on said high k dielectric layer that exposes portions of said high k dielectric layer; and

(c) etching through said exposed portions of said high k dielectric layer with a plasma etch comprised of an inert gas, BCl_3, and one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations.

The MPEP § 2142 provides:

> *... The examiner bears the initial burden of factually supporting any prima facie conclusion of obviousness. If the examiner does not produce a prima facie case, the applicant is under no obligation to submit evidence of nonobviousness...*

It is submitted that, in the present case, the Examiner has not factually supported a prima facie case of obviousness as the references do not teach or suggest all the claim limitations.

Neither Yang nor Ying, either alone or in combination, discloses or suggests etching with a plasma etch comprised of the following combined items:

[1] an inert gas,

[2] BCl_3, and

[3] one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4."

The Examiner alleges that Ying discloses the use of barium trichloride (BCl_3) gases (referring to item designated with reference number [2] above) with other halogens to plasma etch dielectrics at column 3 and thus disclose the features of claims 1 and 20. Applicants respectfully disagree. At column 3, lines 25-55, Ying discloses that "[t]he plasma etchant species are generated from a plasma source (feed) gas comprising boron trichloride (BCl_3) or silicon tetrachloride ($SiCl_4$), or a combination thereof. The BCl_3 or $SiCl_4$ principal etchants are frequently used in combination with argon, oxygen, nitrogen, chlorine, or a combination thereof.

. . .Other essentially inert gases may be added, for example and not by way of limitation, xenon, krypton, or helium." Thus, Ying merely discloses a plasma etchant that comprises BCl_3 or $SiCl_4$ in combination with an inert gas such as argon, oxygen, nitrogen, or chlorine.

Ying does not disclose a plasma etch that comprises item [3] above, i.e., "one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4." There is no disclosure or suggestion in the reference of carbon, hydrogen, or fluorine, let alone one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4. Ying is merely interested in a plasma source gas that comprises BCl_3 and essential inert gases. Ying is not interested in a plasma source gas that comprises one or more fluorocarbon gases $C_XH_YF_Z$. Ying further discloses in the Abstract that other essential inert gases which may be used include xenon, krypton, and helium, and O_2, N_2, or Cl_2 or a combination thereof may be added to increase the etch rate. But nowhere in the reference does Ying disclose or suggest the use of carbon, hydrogen or fluorine in the mixture, let alone the combination thereof. Therefore, Ying does not disclose all of the limitations of claim 1.

Yang also does not disclose all of the limitations of claim 1. The Examiner alleges that Yang discloses the use of fluorine gases in etching high dielectrics at column 12. At column 12, lines 1-10, Yang discloses, "plasma etching the high-K dielectric material, comprises providing a mixture of gases comprising oxygen, a fluorine-containing material and an inert gas. . . .In one embodiment, the fluorine containing material is one or more CF_4, C_2F_6, CHF_3, C_2HF_5, CH_2F_2, $C_2H_2F_4$, XeF_2." However, in this section, Yang merely discloses oxygen, the fluorine-containing material, and the inert gas. Yang does not mention anything about BCl_3. In addition, Yang discloses at column 12, lines 5-6 that "step 1005-d does not use chlorine in the plasma etching." Thus, Yang teaches away from the limitations of claim 1 by specifically teaching that the process does not use Chlorine. Therefore, Yang also does not disclose all of the limitations of claim 1.

Furthermore, the Examiner alleges in "Response to Arguments" of the Final Office Action dated May 11, 2006 that "it is well settled that if two references teach individual components that do similar function, combining the two together would have been well within the level and skills of one of ordinary skill in the art. Thus, it is obvious to one of ordinary skill in the art to combine the gases to etch as claimed. Also, in the etching art, using more than one gas at a time to etch is well known." Appellants respectfully disagree.

There is no teaching or suggestion in either reference that combining BCl_3 and one or more fluorocarbon gases $C_XH_YF_Z$ is well within the level and skill of one of ordinary skill in the art. The Examiner fails to provide any objective reason that suggests the alleged combination. According to MPEP section 2143.01 IV, entitled "Fact That The Claimed Invention Is Within The Capabilities Of One Of Ordinary Skill In The Art Is Not Sufficient By Itself To Establish *Prima Facie* Obviousness," "[a] statement that modifications of the prior art to meet the claimed invention would have been "'well within the ordinary skill of the art at the time the claimed invention was made'" because the references relied upon teach that all aspects of the claimed invention were individually known in the art is not sufficient to establish a *prima facie* case of obviousness without some objective reason to combine the teachings of the references. *Ex parte Levengood*, 28 USPQ2d 1300 (Bd. Pat. App. & Inter. 1993). See also *Al-Site Corp. v. VSI Int'l Inc.*, 174 F.3d 1308, 50 USPQ2d 1161 (Fed. Cir. 1999) (The level of skill in the art cannot be relied upon to provide the suggestion to combine references.). Thus, without some objective reason to combine BCl_3 and one or more fluorocarbon gases $C_XH_YF_Z$, the Examiner cannot rely on the ground that the alleged combination is well within the level of one in ordinary skill in the art in the rejection claim 1.

In addition, neither Yang nor Ying, either alone or in combination, discloses or suggests the alleged combination. While Ying discloses plasma etchant species that are generated from a plasma source gas comprising BCl_3, Ying does not disclose or suggest a plasma source gas that includes one or more fluorocarbon gases $C_XH_YF_Z$. On the other hand, Yang discloses a plasma etchant that comprises oxygen, fluorine-containing material and an inert gas. But there is no mention of BCl_3 anywhere in the reference. For at least this reason, Yang and Ying fail to render claim 1 *prima facie* obvious.

Moreover, the Ying reference, by providing that no chlorine is used in the plasma etching process, clearly teaches away from the alleged combination. Thus, for this reason alone, the Examiner's burden of factually supporting a *prima facie* case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

Additionally, § 2142 of the MPEP also provides:

> *...the examiner must step backward in time and into the shoes worn by the hypothetical 'person of ordinary skill in the art' when the invention was unknown and just before it was made.....The examiner must put aside knowledge of the applicant's disclosure, refrain from using hindsight, and consider the subject matter claimed 'as a whole'.*

Here, neither Yang nor Ying teaches, or even suggests, the desirability of the combination since neither teaches "etching through said exposed portions of said high k dielectric layer with a plasma etch comprised of an inert gas, BCl_3, and one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4" as specified above and as claimed in claim 1.

Thus, it is clear that neither reference provides any incentive or motivation supporting the desirability of the combination. Therefore, there is simply no basis in the art for combining the references to support a 35 U.S.C. § 103 rejection.

In this context, the MPEP further provides at § 2143.01:

> *The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination.*

In the above context, the courts have repeatedly held that obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention, absent some teaching, suggestion or incentive supporting the combination. In the present case it is clear that the Examiner's combination arises solely from hindsight based on the invention without any showing, suggestion, incentive or motivation in either reference for the combination as applied to claim 1. Appellants submit that the Examiner has simply taken unrelated phrases from the various references and combined them using Appellants' disclosure as a blueprint without any teaching or suggestion in the references themselves.

The case law forbids this type of combination by requiring that there must be evidence that a skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. It is also clear that a rejection cannot be predicated on the mere identification of individual components of claimed limitations. Rather, particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention,

would have selected these components for combination in the manner claimed. *Ecolochem Inc. v. Southern California Edison*, 56 USPQ2d 1065, 1076 (Fed. Cir. 2000).

Furthermore, Appellants respectfully submit that the Final Office Action simply takes bits and pieces of information from each reference and pieces them together like a jigsaw puzzle using the Appellants' disclosure as a blueprint. However, the case law makes it clear that the best defense against hindsight-based obviousness analysis is the rigorous application of the requirement for a showing of a teaching or motivation to combine the prior art references. See *Dembiczak*, 50 USPQ2d, 1614, 1617 (Fed. Cir. 1999). "Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability – the essence of hindsight." *Id.* It is respectfully submitted that the only way the cited references could be pieced together to defeat patentability is indeed to use Appellants' disclosure as a blueprint. For at least this reason, Yang and Ying fail to render claim 1 *prima facie* obvious

Independent claim 20 recites similar features as claim 1. Claims 2-19 and 21-40 depend from, and further limit, claims 1 and 20. Therefore, the same distinctions between Yang and Ying and the claimed invention in claims 1 and 20 applies for claims 2-19 and 21-40. For at least this reason, the Examiner has failed to provide a prima facie case of obviousness with regard to claims 2-19 and 21-40.

In addition, neither Yang nor Ying, either alone or in combination, discloses or suggests the specific features of claims 2-19 and 21-40. For example, neither Yang nor Ying discloses or suggest "wherein said plasma etch is performed with BCl_3, an inert gas comprised of Ar, He, Ne, or Xe, and one or more fluorocarbon gases including CF_4, CHF_3, CH_2F_2, CH_3F, C_2HF_5, $C_2H_2F_4$ and C_2F_6," as recited in claims 10 and 29. As discussed above, neither Yang nor Ying discloses the combination of BCl_3 and one or more fluorocarbon gases. Yang merely discloses a plasma source gas that comprises BCl_3 and inert gases. On the other hand, Ying discloses a plasma etching process that comprises fluorine-containing material and inert gases, but specifically teaches away from the use of chlorine. Therefore, neither Yang nor Ying discloses a plasma etch with BCl_3, inert gases and one or more fluorocarbon gases, let alone inert gas comprise of Ar, He, Ne, or Xe, or one or more fluorocarbon gases including CF_4, CHF_3, CH_2F_2, CH_3F, C_2HF_5, $C_2H_2F_4$ and C_2F_6. Thus, for this reason alone, the Examiner's burden of factually supporting a

prima facie case of obviousness has clearly not been met, and the rejection under 35 U.S.C. §103 should be withdrawn.

Conclusion

Accordingly, it is respectfully submitted that the references alone or in combination do not disclose or suggest the subject matter of claims 1-40.

For all of the foregoing reasons, it is respectfully submitted that claims 1-40 be allowed. A prompt notice to that effect is respectfully requested.

Respectfully submitted,

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Dated: October 16, 2006

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CLAIMS APPENDIX

1. A method of removing a high k dielectric layer from a substrate comprising the steps of:

(a) providing a substrate with a high k dielectric layer formed thereon;

(b) depositing a gate layer and forming a gate electrode on said high k dielectric layer that exposes portions of said high k dielectric layer; and

(c) etching through said exposed portions of said high k dielectric layer with a plasma etch comprised of an inert gas, BCl_3, and one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4.

2. The method of claim 1 wherein said plasma etch is further comprised of a low bias power of about 10 to 50 Watts.

3. The method of claim 1 wherein said high gate dielectric layer is formed by a chemical vapor deposition (CVD), metal organic CVD (MOCVD), or an atomic layer deposition (ALD) process and has a thickness between about 15 and 100 Angstroms.

4. The method of claim 1 wherein said high k dielectric layer is comprised of one or more of HfO_2, ZrO_2, Ta_2O_5, TiO_2, Al_2O_3, Y_2O_3 or La_2O_5.

5. The method of claim 1 wherein the high k dielectric layer is a silicate, aluminate, nitride, or oxynitride of Hf, Zr, Ta, Ti, Y, or La.

6. The method of claim 1 wherein the high k dielectric layer is subjected to a post-deposition surface treatment or an anneal step prior to forming a gate layer on said high k dielectric layer.

7. The method of claim 6 wherein said anneal step is comprised of heating the substrate in an O_2 of H_2 ambient at about 800°C for a period of about 20 minutes.

8. The method of claim 1 wherein said gate layer is comprised of polysilicon, amorphous silicon, Si-Ge, W, Ta, Al, Ti, Ni, Ru, Pa, Pt, Mo, TiN, TaN, or TaSiN.

9. The method of claim 1 wherein said gate layer has a thickness between about 500 and 1500 Angstroms.

10. The method of claim 1 wherein said plasma etch is performed with BCl_3, an inert gas comprised of Ar, He, Ne, or Xe, and one or more fluorocarbon gases including CF_4, CHF_3, CH_2F_2, CH_3F, C_2HF_5, $C_2H_2F_4$ and C_2F_6.

11. The method of claim 1 wherein said plasma etch is performed with a BCl_3 flow rate of about 100 to 400 standard cubic centimeters per minute (sccm), a fluorocarbon gas flow rate from about 5 to 20 sccm, and an inert gas flow rate between about 100 and 500 sccm.

12. The method of claim 1 wherein said plasma etch is performed with a chamber pressure from about 5 to 20 mTorr and a substrate temperature between about 50°C and 70°C.

13. The method of claim 1 wherein said plasma etch is performed with an RF power between about 200 and 800 Watts.

14. The method of claim 1 wherein said plasma etch is continued until an end point is reached as indicated by a drop in an OES signal for a metal in the high k dielectric layer or is carried out for a period of about 60 to 90 seconds.

15. The method of claim 1 further comprised of forming an interfacial layer that is SiO_2, silicon nitride, or silicon oxynitride on said substrate prior to forming said high k dielectric layer.

16. The method of claim 15 wherein said interfacial layer is removed during the same plasma etch step that removes the high k dielectric layer.

17. The method of claim 1 wherein said high k dielectric layer is etched at a rate that is more than about ten times the etch rate of said gate electrode under the same conditions.

18. The method of claim 1 further comprised of a wet clean step after the plasma etch through the high k dielectric layer is complete.

19. The method of claim 1 further comprised of forming a spacer on opposite sides of said gate electrode before etching through said high k dielectric layer.

20. A method of forming a MOSFET, comprising:

(a) providing a substrate having shallow trench isolation features which separate active regions;

(b) forming a high k dielectric layer on said substrate;

(c) depositing a gate layer on said high k dielectric layer and etching through said gate layer to form a gate electrode and expose portions of said high k dielectric layer, said gate electrode is aligned over an active region; and

(d) etching through exposed portions of said high k dielectric layer with a plasma etch comprised of an inert gas, BCl_3, and one or more fluorocarbon gases $C_XH_YF_Z$, wherein x and z are integers and y is an integer or is 0, or CH_4.

21. The method of claim 20 wherein step (d) is further comprised of a low bias power of about 10 to 50 Watts.

22. The method of claim 20 wherein said high k dielectric layer is formed by a CVD, MOCVD, or ALD process and has a thickness between about 15 and 100 Angstroms.

23. The method of claim 20 wherein said high k dielectric layer is comprised of one or more of HfO_2, ZrO_2, Ta_2O_5, TiO_2, Al_2O_3, Y_2O_3 or La_2O_5.

24. The method of claim 20 wherein said high k dielectric layer is a silicate, aluminate, nitride, or oxynitride of Hf, Zr, Ta, Ti, Y, or La.

25. The method of claim 20 wherein the high k dielectric layer is subjected to a post-deposition surface treatment or an anneal step prior to forming a gate layer on said high k dielectric layer.

26. The method of claim 25 wherein said anneal step is comprised of heating the substrate in an O_2 or H_2 ambient at about 800°C for a period of about 20 minutes.

27. The method of claim 20 wherein said gate layer is comprised of polysilicon, amorphous silicon, Si-Ge, W, Ta, Al, Ti, Ni, Ru, Pa, Pt, Mo, TiN, TaN, or TaSiN.

28. The method of claim 20 wherein said gate layer has a thickness between about 500 and 1500 Angstroms.

29. The method of claim 20 wherein said etching through exposed portions of said high k dielectric layer is performed with BCl_3, an inert gas comprised of Ar, He, Ne, or Xe, and one or more $C_XH_YF_Z$ gases including CF_4, CHF_3, CH_2F_2, CH_3F, C_2HF_5, $C_2H_2F_4$, and C_2F_6.

30. The method of claim 20 wherein said etching through exposed portions of said high k dielectric layer is performed with a BCl_3 flow rate of about 100 to 400 sccm, a fluorocarbon gas flow rate from about 5 to 20 sccm, and an inert gas flow rate between about 100 to 500 sccm.

31. The method of claim 20 wherein said etching through exposed portions of said high k dielectric layer is performed with a chamber pressure from about 5 to 20 mTorr and a substrate temperature between about 50°C and 70°C.

32. The method of claim 20 wherein said etching through exposed portions of said high k dielectric layer is performed with an RF power between about 200 and 800 Watts.

33. The method of claim 20 wherein said etching through exposed portions of said high k dielectric layer is continued until an end point is reached as indicated by a drop in an OES signal for a metal in the high k dielectric layer or is carried out for a period of about 60 to 90 seconds.

34. The method of claim 20 further comprised of forming an interfacial layer comprised of silicon nitride, SiO_2, or silicon oxynitride on said substrate prior to forming said high k dielectric layer.

35. The method of claim 34 wherein said interfacial layer is removed by the same plasma etch that etches through exposed portions of said high k dielectric layer.

36. The method of claim 20 wherein said etching through exposed portions of said high k dielectric layer is performed in the same etch chamber as etching through the gate layer.

37. The method of claim 20 wherein said etching through the exposed portions of said high k dielectric layer is performed at a rate that is more than about ten times the etch rate of said gate electrode under the same conditions.

38. The method of claim 20 further comprised of a wet clean step after etching through exposed portions of said high k dielectric layer is complete.

39. The method of claim 20 further comprised of forming a spacer on opposite sides of said gate electrode before etching through exposed portions of said high k dielectric layer.

40. The method of claim 20 further comprised of forming source/drain regions in said substrate and forming a silicide layer on the gate electrode and on source/drain regions in said substrate.

EVIDENCE APPENDIX

There is no evidence regarding the above-identified patent application.

RELATED PROCEEDINGS APPENDIX

There is no related proceeding regarding the above-identified patent application.